CMOS COMPATIBLE HERMETIC WAFER LEVEL PACKAGING FOR INERTIAL MEMS

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INTRODUCTION

Recently, there has been an increased demand for MEMS devices where the MEMS structure is integrated with CMOS circuitry at wafer level. Such devices could be fabricated in a conventional foundry using CMOS compatible materials in the manufacturing process. Currently, wafer level packaging of inertial MEMS devices either involves traditional glass frit or metal systems involving gold eutectic which is expensive and not compatible with CMOS front-end processing. The use of Al as a bonding metal is compatible with CMOS integration since Al is already used as a bond pad metal and has no contamination concerns in a standard CMOS clean room environment. Al-Ge based eutectic wafer bonding has been shown to provide a practical solution for MEMS-CMOS integration and hermetic wafer level packaging due to both Al and Ge being CMOS fab friendly, electrically conductive and orders of magnitude less permeable than glass.

This applications note describes a practical Al-Ge bonding process where Al is used as a seal ring metal on the MEMS device wafers while Ge is used as a cap wafer material. The Aluminum-Germanium system [2,3] is a simple eutectic system with three phases (a) liquid (b) fcc (Al) solid solution and (c) diamond cubic (Ge) solid solution as shown in Figure 1. The eutectic point of this system has not been reliably reported but most published data points at a eutectic point of 420°C ± 4°C (J Phase Equil. 19(1), 1998)

For Al-Ge bonding, the thickness of the stack as well as the seal ring geometries should be designed while taking into account the expected atomic percentage of Ge at the interface. In addition for this process, care needs to be taken to ensure that the Al and Ge surfaces are free of native oxides and organic contamination from previous DRIE and lithography steps. One of the common methods to clean Ge deposited substrates is to dip the wafers in a dilute HF BOE solution. In addition, forming gas (3-5% H\textsubscript{2}) is used as an overpressure gas to avoid oxide growth inside the bonder prior to substrates coming in contact.

PROCESS SETUP

This study used 200 mm single side...
polished (100) silicon wafers for the substrate material. Figure 2 shows the SEM cross-sections of the deposited film stacks prepared for blanket AlGe bonding. As a starting point, blanket Al/Ge deposited wafers with 0.1 μm TEOS/0.5 μm Ge /1.5 μm Al were bonded to varying thickness Ge deposited on Si wafers to qualify the bond process.

Once the bond process was proven on the blanket pairs, patterned wafers were used to optimize the process and to reduce eutectic squeeze out. For aligned wafer bonding preparation, the Si cap wafer had patterned 5 - 10kÅ Ge with varying seal ring widths while the device wafer was deposited and patterned with 10kÅ Al plus 5 - 10kÅ Ge on top (Figure 3). The seal ring widths varied from 10μm to 200μm. Both device and cap wafers had front side targets and were aligned using SUSS MicroTec BA200 bond aligner inter-substrate alignment method in which the microscopes move in between the substrates for face to face alignment.

During the alignment process, 100μm - 200μm thick spacers were inserted between the substrates prior to clamping to allow the flow of forming gas and consequently to pull precise vacuum between the substrates prior to bonding. Once aligned, the wafers were clamped on the bond fixture and transferred to a SUSS MicroTec CB200 wafer bonder.

Forming gas (95%N₂, 5%H₂) was used as the process gas while N₂ was used as the purge gas. During the bonding cycle, the bond chamber was pumped down to base vacuum at 350°C - 390°C, followed by introduction of forming gas in overpressure (2 bar abs). After the forming gas step, the bond chamber went through a final pump-down step. The two substrates to be bonded were separated by spacers until the final pump-down step. After the chamber reached the specified vacuum level, the spacers were removed via sequential spacer removal process and a uniform force was applied on the substrates. The temperature was then elevated to 5 - 30°C above the AlGe eutectic point under force.

For these experiments, the bonding conditions were varied from 420°C to 455°C for the bond temperature, while the applied force and bond time varied from 15 - 50 KN and 2 - 30 minutes respectively. The typical bonder process profile for AlGe bonding from CB200 is shown in Figure 4. Post bond alignment was measured using an offline transmission IR (infrared) microscope. Post bonding, the bond interface was evaluated via scanning acoustic microscopy (SAM). To further investigate the bond interface, cross-sections of the samples were analyzed via Scanning Electron Microscopy.
RESULTS & DISCUSSION

SAM & IR ANALYSIS:
Void-free bonding (SAM) for both blanket as well as patterned substrates with good post bond alignment (<3 μm post bond) was observed in the temperature range 435°C - 445°C and tool force range of 20kN - 40kN. Figure 5 shows the high resolution SAM image of a section of a patterned Al-Ge pair showing bonded seal rings with varying seal widths. Figure 6 compares the squeeze-out of the eutectic alloy from two Al-Ge runs processed at 440°C and 455°C respectively. At temperatures above 445°C, eutectic squeeze-out was observed irrespective of the tool force used owing to excessive melting while minimal squeeze-out was observed at temperatures up to 440°C. In addition, at temperature >445°C, post bond misalignment >5 μm was observed which is attributed to the molten eutectic state and therefore slippage at the bond interface. Mixed bonding was observed in the 425-440°C range with moderate tool force (20kN - 30kN) while poor bonding was observed below 425°C irrespective to tool force up to 50kN. Figure 7 shows the transmission IR images of seal rings taken with an offline microscope and depict void free bonding and no eutectic squeeze-out with post bond alignment <3 μm. X-section and plan SEM analysis of the bonded pairs shown in Figure 8 shows Ge dendrites within an Al matrix due to low solubility between Al and Ge.

CONCLUSION AND ONGOING WORK
This application note described an optimized Al-Ge based bonding process for CMOS friendly wafer level packaging that can be easily integrated into MEMS wafer level packaging line. The integration of this process with a fusion bonding is also being actively investigated as shown in Figure 9. Ongoing process development is geared towards optimizing this process for high throughput and yield in a production environment. With optimization of pre-cleaning techniques, it is hoped that the process temperature and forces can be further reduced.

References


THE AUTHOR

Sumant Sood is Senior Applications Engineer for Wafer Bonders at SUSS MicroTec. His recent experience includes permanent and temporary wafer bonding process development for MEMS, LEDs and 3-D integration applications. He has authored more than 20 papers in wafer bonding and related areas. He received his B.Tech in Electrical Engineering from India and MS in Microelectronics from University of Central Florida. Sumant is a member of SEMI Standards committee on 3DS-C and MEMS/NEMS and is a senior member of the IEEE.

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